

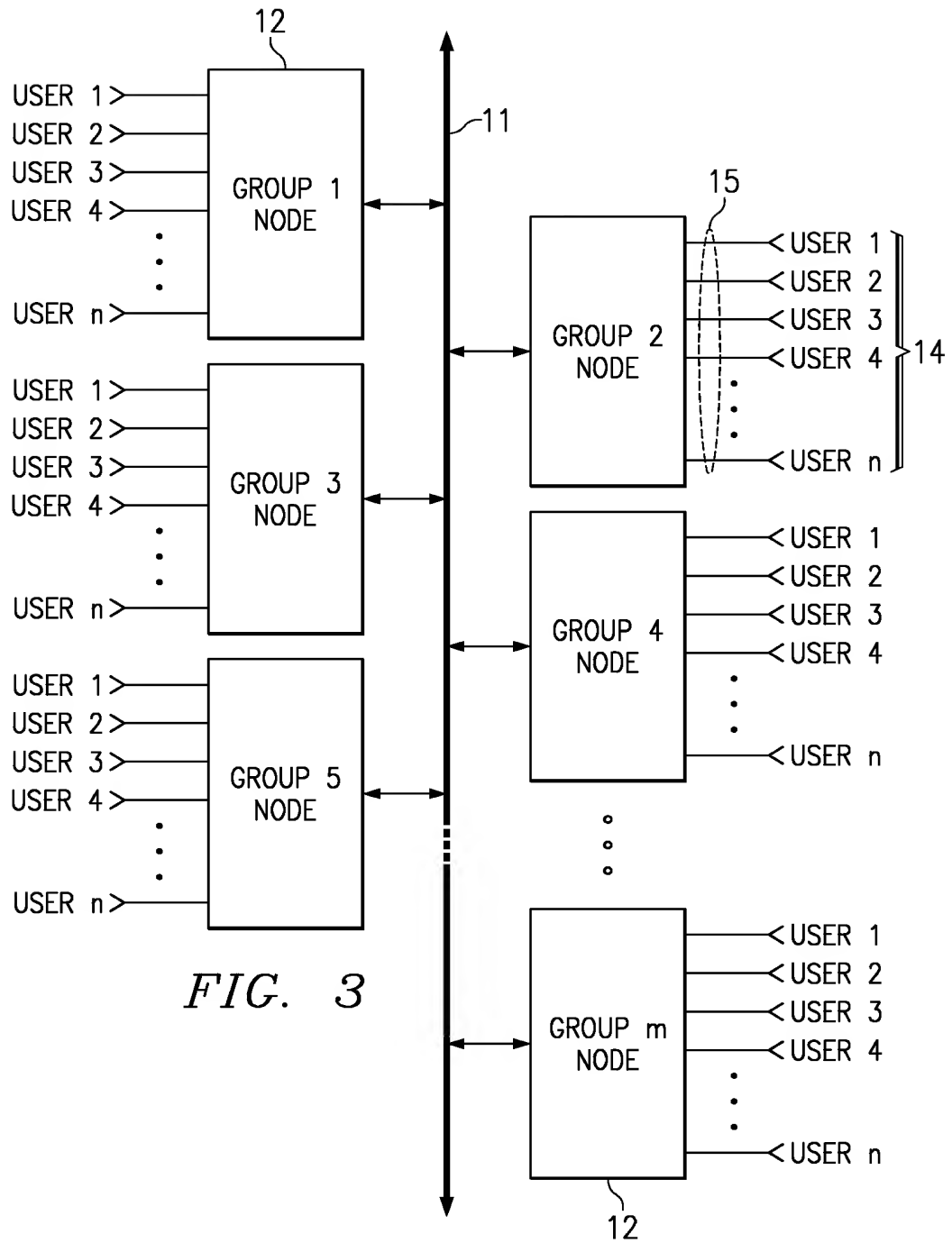
FIG. 1
(PRIOR ART)

The diagram illustrates a prior art system architecture. A central vertical line, labeled 3, represents a communication bus. On the left side of the bus, there are four nodes: 'LOCATION 1 NODE', 'LOCATION 3 NODE', 'LOCATION 5 NODE', and 'LOCATION n NODE'. Each node consists of a 'MUX/DEMUX' block connected to a telephone handset icon. A 'CENTRAL PROCESSOR' block, labeled 6, is connected to the bus via multiple bidirectional arrows. On the right side of the bus, there are three nodes: 'LOCATION 2 NODE', 'LOCATION 4 NODE', and 'LOCATION n NODE'. Each node also consists of a 'MUX/DEMUX' block connected to one or more telephone handset icons. The bus line 3 has a break in the middle, indicated by two short parallel lines.

LOCATION n NODE

FIG. 2
(PRIOR ART)

BITS		
15	8 7 0	
PARTICIPANT 1	SAMPLE 2	SAMPLE 1
	SAMPLE 4	SAMPLE 3
PARTICIPANT 3	SAMPLE 2	SAMPLE 1
	SAMPLE 4	SAMPLE 3
PARTICIPANT 5	SAMPLE 2	SAMPLE 1
	SAMPLE 4	SAMPLE 3
⋮		
GROUP n	SAMPLE 2	SAMPLE 1
	SAMPLE 4	SAMPLE 3



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